In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 to 12. (Cancelled).

13. (Previously Presented) An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal;

a digital to analog converter connected to the output terminal operable to convert the channel of PCM data to an analog audio signal on a D/A output terminal;

a speaker subsystem connected to the D/A output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion

of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

14. (Original) The audio reproduction system of Claim 13, wherein the means for acquiring comprises a satellite broadcast receiver.

15. (Original) The audio reproduction system of Claim 13, wherein the means for acquiring comprises a digital disk player.

16. (Original) The audio reproduction system of Claim 13, wherein the means for acquiring comprises a cable TV receiver.

17. (Previously Presented) The system of Claim 13, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

18. (Previously Presented) The system of Claim 13, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

19. (Previously Presented) The system of Claim 18, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

20. (Previously Presented) The system of Claim 19, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.

21. (Previously Presented) An audio reproduction system, comprising:

means for acquiring a stream of data which contains encoded audio data;

a data device for processing the stream of data connected to the means for acquiring, the data device operable to form at least one channel of PCM data on an at least one device output terminal; and

wherein the data device further comprises:

an instruction register operable to hold an instruction during processing by the data processing device;

a central processing unit (CPU) operationally connected to the instruction register and operable to process a data word in response to the instruction;

an index register operationally connected to the instruction register and operable to provide a first address in response to the instruction; and

address circuitry operable to form a memory address of the data word by selecting a first portion of the first address from the index register and combining the first portion of the first address with a first portion of an immediate field selected from the instruction, such that the first portion of the immediate field is a most significant address portion with the first portion of the first address as a least significant address portion, wherein the first portion of the immediate field has a first width and the first portion of the first address has a second width.

22. (Previously Presented) The system of Claim 21, wherein the address circuitry is operable to form the memory address by concatenating the first portion of the immediate field as a most significant address portion with the first portion of the first address as a least significant address portion.

23. (Previously Presented) The system of Claim 21, the data device further comprising decoding circuitry connected to the address circuitry and operable to select a first value for the first width from a first range of values responsive to the instruction.

24. (Previously Presented) The system of Claim 23, wherein the decoder circuitry is further operable to select a second value for the second width from a second range of values responsive to the instruction.

25. (Previously Presented) The system of Claim 24, wherein the decoder circuitry is further operable to parse the immediate field to determine a bit position for a first toggled bit.